

IN THE CLAIMS

Claim 1. (Cancelled).

Claim 2. (Canceled).

Claim 3. (Currently Amended) The delay time adjusting circuit as claimed in claim [[1]] 7, wherein said ~~comparing means~~ phase comparison circuit supplies a signal indicating said comparison result to said ~~adjusting means~~ delay adjusting circuit according to said signal generated by said ~~second dividing means~~ divider.

Claims 4 to 6. (Cancelled).

Claim 7. (New) A delay time adjusting circuit receiving an input signal for outputting an output signal by adjusting a delay time of said input signal, comprising:

a first divider configured to divide a frequency of said input signal by a first division rate;

a variable delay circuit, including a delay chain in which delay units are coupled in series, configured to delay said input signal by selecting a number of said delay units to output said output signal;

a second divider configured to divide a frequency of said output signal by a second division rate higher than said first division rate;

a phase comparison circuit configured to compare phases of signals from said first and second dividers; and

a delay adjusting circuit configured to select the number of said delay units in response to a comparison result in said phase comparison circuit.

Claim 8. (New) A delay time adjusting circuit receiving an input signal for outputting an output signal by adjusting a delay time of said input signal, comprising:

a variable delay circuit, including a delay chain in which delay units are coupled in series, configured to delay said input signal by selecting a number of said delay units to output said output signal;

a divider configured to divide a frequency of said output signal by a division rate, wherein a frequency of a signal from said driver is less than a frequency of said input signal;

a phase comparison circuit configured to compare phases of said input signal and said signal from said divider; and

a delay adjusting circuit configured to select the number of said delay units in response to a comparison result in said phase comparison circuit.

Claim 9. (New) A delay time adjusting method for receiving an input signal and outputting an output signal by adjusting a delay time of said input signal, comprising the steps of:

- (a) dividing a frequency of said input signal by a first division rate;
- (b) using a delay chain in which delay units are coupled in series and delaying said input signal by selecting a number of said delay units to output said output signal;

(c) dividing a frequency of said output signal by a second division rate higher than said first division rate;

(d) comparing phases of signals obtained by said steps (a) and (c); and

(e) selecting the number of said delay units in response to a comparison result in said step (d).

Claim 10. (New) A delay time adjusting method for receiving an input signal and outputting an output signal by adjusting a delay time of said input signal, comprising the steps of:

(a) using a delay chain in which delay units are coupled in series and delaying said input signal by selecting a number of said delay units to output said output signal;

(b) dividing a frequency of said output signal by a division rate, wherein a frequency of a signal from said divider is less than a frequency of said input signal;

(c) comparing phases of said input signal and said signal obtained by said step (b); and

(d) selecting the number of said delay units in response to a comparison result in said step (c).

Claim 11. (New) The delay time adjusting method as claimed in claim 9, wherein said step (d) supplies a signal indicating said comparison result to said step (e) according to said signal generated by said step (c).